AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

storing instructions for sending interrupt controller initializing data to a first interrupt controller;

storing instructions for re-routing interrupt controller initializing data to a second interrupt controller;

sending interrupt controller initializing data to ~~a~~ the first interrupt controller;

re-routing the interrupt controller initializing data to ~~a~~ the second interrupt controller; and

configuring the second interrupt controller to manage interrupts of at least a first interrupt type.

2. (Previously Presented) The method of claim 1, further comprising:

configuring a system management interrupt to recognize interrupt controller initializing data for the first interrupt controller.

3. (Previously Presented) The method of claim 1, further comprising:

configuring a system management interrupt to recognize interrupt controller initializing data; and

re-routing interrupt controller initializing data to the second interrupt controller starting from a first command word,

wherein interrupt controller initializing data comprises a plurality of command words including the first command word that begins the initializing of the first interrupt controller.

4. (Previously Presented) The method of claim 1, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

5. (Currently Amended) A machine readable storage media containing executable program instructions which when executed cause a digital processing system to perform a method comprising:

storing instructions for sending interrupt controller initializing data to a first interrupt controller;

storing instructions for re-routing interrupt controller initializing data to a second interrupt controller;

sending interrupt controller initializing data to ~~a~~ the first interrupt controller;

re-routing interrupt controller initializing data to ~~a~~ the second interrupt controller; and

configuring the second interrupt controller to manage interrupts of a first interrupt type.

6. (Previously Presented) The media of claim 5, further comprising:

configuring a system management interrupt to recognize interrupt controller initializing data for the first interrupt controller.

7. (Previously Presented) The media of claim 5, further comprising:

configuring a system management interrupt to recognize interrupt controller initializing data; and

re-routing interrupt controller initializing data to the second interrupt controller starting from a first command word,

wherein interrupt controller initializing data comprises a plurality of command words including the first command word that begins the initializing of the first interrupt controller.

8. (Previously Presented) The media of claim 5, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

9. (Previously Presented) A system comprising:

a central processing unit (CPU);

a first bus coupled to the CPU;

a first interrupt controller, coupled to the first bus, operable to manage communication with the CPU of interrupts of a first interrupt type;

a second bus coupled to the CPU;

a second interrupt controller, coupled to the second bus and to the first interrupt controller, operable to manage communication with the CPU of interrupts of a second interrupt type; and

a memory coupled to the second interrupt controller comprising a computer-readable medium having a computer-readable program embodied therein for directing operation of the system, the computer-readable program comprising:

instructions for managing interrupts of the first interrupt type by the second interrupt controller, exclusive of the first interrupt controller;

instructions for sending interrupt controller initializing data to the first interrupt controller to initialize the first interrupt controller;

instructions for re-routing interrupt controller initializing data to the second interrupt controller to initialize the second interrupt controller; and

instructions for configuring the second interrupt controller to manage interrupts of the first interrupt type.

10. (Cancelled)

11. (Previously Presented) The system of claim 9, wherein the instructions for re-routing interrupt controller initializing data comprise:

instructions for configuring a system management interrupt to recognize interrupt controller initializing data related to at least the first interrupt type.

12. (Previously Presented) The system of claim 9, wherein interrupt controller initializing data comprises a plurality of command words and a first command word begins the initializing of the first interrupt controller, and the computer-readable program comprises instructions for configuring a system management interrupt to recognize initializing data related to at least the first interrupt type and re-route initializing data to the second interrupt controller from the first command word.

13. (Previously Presented) The system of claim 9, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises an advanced programmable interrupt controller.

14. (Cancelled)

15. (Currently Amended) A system comprising:

a central processing unit (CPU);

first means of interrupt processing for managing communication with the CPU of interrupts of a first interrupt type;

second means of interrupt processing for managing communication with the CPU of interrupts of a second interrupt type;

means for routing interrupts of the first interrupt type to the second interrupt processing means;

means for sending interrupt controller initializing data to the first interrupt processing means;

means for re-routing interrupt controller initializing data to the second interrupt processing means; ~~and~~

means for managing interrupts of the first interrupt type by the second interrupt processing means exclusive of the first interrupt processing means;

means for storing instructions for sending interrupt controller initializing data to a first interrupt controller; and

means storing instructions for re-routing interrupt controller initializing data to a second interrupt controller.